A 400 × 400 3.24 µm 117 dB Dynamic Range 3-layer Stacked Digital Pixel Sensor with Triple Quantization and Fixed Pattern Noise Correction

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***Abstract*—This paper presents a 400 × 400 digital pixel sensor (DPS) with the smallest 3.24 µm pixel size is developed in a 45nm/40nm/40nm three-layer stacked process. The sensor achieves a single-exposure 117 dB dynamic range (DR) incorporated with the overlapped triple quantization (3Q) and fixed pattern noise correction (FPN-C) while the noise floor of 4.4 e^-_{rms} and a dark FPN of 2.4 e^-_{rms}. This work consumes 3.06 mW at 30 fps with a FoM of 0.0049 e^-_{rms} × pJ and the die size of 2.47 × 1.85 mm^2. This work is developed for high DR (HDR), low power consumption, and small form fact to meet the growing demands of augmented reality (AR) and virtual reality (VR) devices.**

***Index Terms*— Digital pixel sensor (DPS), in-pixel ADC, stacked process, 3D-IC, high dynamic range, (HDR), triple quantization (3Q), fixed pattern noise (FPN), fixed pattern noise correction (FPN-C), lateral overflow integration capacitor (LOFIC), image signal processing (ISP), sparse transmission (ST), transmission map (TM), augmented reality (AR), and virtual reality (VR).**

I. Introduction

In recent years, with the aid of the stacked process, digital pixel sensor (DPS) has been developed for augmented reality (AR) glasses and virtual reality (VR) headsets with the advantage of low power consumption, high dynamic range (HDR) with the overlapped triple quantization (3Q), and global shutter in a small pixel [1] - [3]. In the two-layer stacked prior arts [2], [3], the peripheral analog modules, macros and digital logics in the bottom layer lead to the area overhead that the top layer is required to allocate the same area overhead outside of the pixel array without active devices for chip stacking. The utilization rate of digital logics is not good due to placing and routing in the odd surrounding area, which makes the area overhead in the top layer become significant large. This work incorporates the three-layer stacked process by moving all the macros and digital logics from the middle layer to the third (bottom) layer which improves the utilization rate of macros and digital circuits and saves the area overhead in the top layer. With the compactness in full-digital bottom layer, the on-chip functionalities are embedded such as fixed pattern noise correction (FPN-C) with the off-array pixel FPN memory to cancel FPN in the linear ADC modes (PD-ADC and FD-ADC), image signal processer (ISP) with high dynamic range (HDR) processor to linearize 3Q codes and defect pixel correction (DPC) to correct defect pixel, and sparse transmission (ST) with all data processed on-chip and only the necessary data being transmitted. Moreover, the pixel size is reduced to 3.24 µm by adopting a single-ended comparator merged with the 3Q logics.

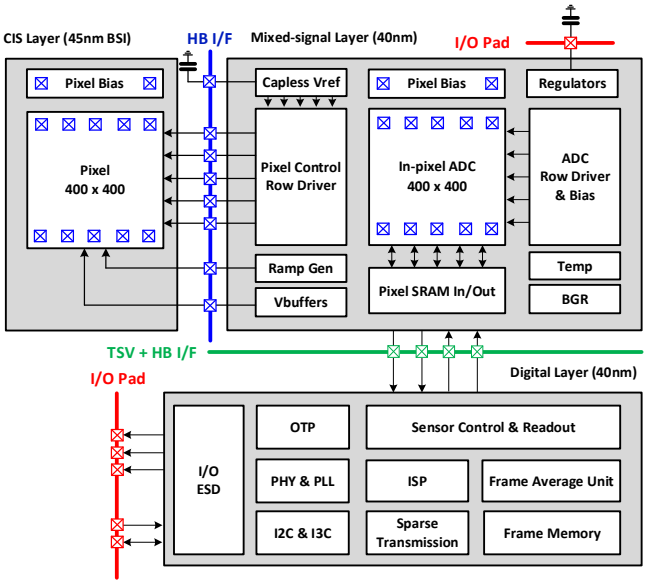

Fig. 1. The sensor architecture and functional blocks in three layers.

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To meet the growing demands for compact form factor and performance requirements of AR/VR devices, this work presents a small form-factor three-layer stacked global shutter DPS. The 2.47 × 1.85 mm^2 sensor chip has an effective 400 × 400 pixel array in the smallest 3.24 µm pixel, which is essential for creating appealing and light-weight AR/VR devices.

II. Architecture

To achieve a more compact and aggressive small form-factor in module, minimizing power rails is essential. Hence, the three-layer stacked sensor is implemented in near process nodes (45nm/40nm/40nm) to share three power rails of 2.6V, 1.8V and 1.1V as shown in Fig. 1. The top layer (CIS, 45 nm) comprises the pixel array with backside illumination (BSI) process and near-infrared (NIR) enhanced technology to boost quantum efficiency (QE) in the NIR spectrum. The middle layer (Mixed-signal, 40 nm) contains an in-pixel analog-to-digital converter (ADC) array with analog peripheral and control circuits. On-chip reference buffer (in the middle layer) and capacitors (in the peripheral area of the top layer) are implemented for pixel controls to save the pin counts and external discrete capacitors. All digital logics, including macros (PLL, PHY, and OTP) and memories, are implemented in bottom layer (Digital, 40 nm) for a compact, digital-only integration. In the three-layer stacked process as illustrated in Fig. 2, the top and middle layers are directly connected via Cu-Cu hybrid bonds (HBs). Similarly, the middle and bottom layers are connected via HBs and corresponding through-silicon vias (TSVs) on the substrate of the middle layer.

III. Pixel Schematic and Operation

Fig. 3 shows the schematic of pixel, in-pixel ADC, and the 3Q timing [1] – [4]. The pixel comprises a photodiode, an anti-blooming gate (AB), and 4T + 1C lateral overflow integration capacitor (LOFIC) readout. The 3Q scheme sequentially operates (1) time-to-saturation (TTS) mode (8-b, high-illuminance): the ADC operates time counting with a AC-coupled reference threshold to detect the overflow charge (downward V_{SF}) during exposure; linear ADC modes of (2) PD-ADC (9-b, low-illuminance) and (3) FD-ADC (8-b, medium-illuminance): the ADC functions as a single-slope ADC with a downward ramp (V_{RAMP}) to covert the corresponding PD and FD signals, respectively. With the state latch (D-latch controlled by CHK), SRAM bank locks the digital ramp data (Gray code) when the comparator flips without any flipping from the precedent operations. The stored digital code from 3Q operation is read out from the ADC pixel array and processed by the on-chip ISP before transmission.

The in-pixel ADC comprises a single-ended comparator with AC-coupled input 3D-MIM (metal-insulator-metal) capacitors (C_{IN} and C_{INR}) without occupying the backend of line (BEOL),

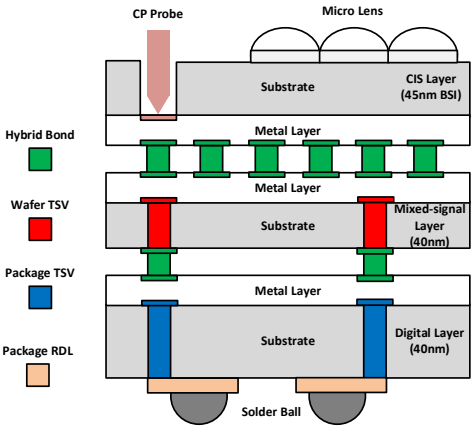

Fig. 2. The cross-section of three-layer stacked sensor.

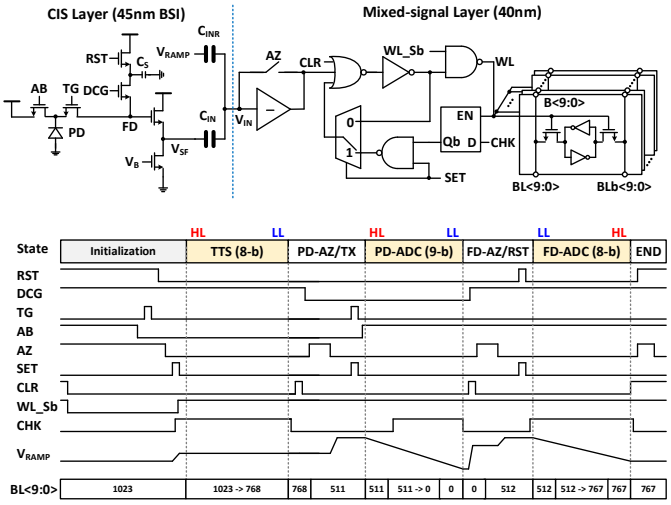

Fig. 3. The pixel and in-pixel ADC schematic and operation timing.

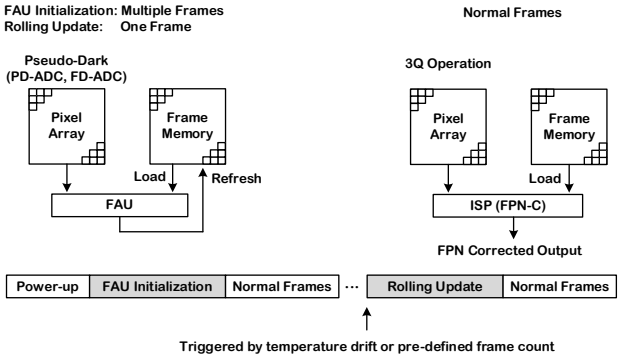

Fig. 4. The operation of FAU and FPN-C.

along with 3Q logics and 10-b SRAM memory. The AC-coupled input network allows the power domain of in-pixel ADC decoupled from pixel and V_{RAMP}, and ADC is able to fully utilize the advantages of core-voltage devices including low power, area scaling, and single voltage domain integration with 3Q logics and SRAM. To maximize the signal power and hence signal-to-noise ratio (SNR), the C_{IN} : C_{INR} are 2:1 with unit-

element matching of 3D-MIM capacitors at the cost of larger V_{RAMP} swing, which can be easily achieved in AC-coupled input network by generating V_{RAMP} in high power supply voltage (2.6V). This approach also fixes the comparator flipping DC level determined by auto-zeroing, thereby eliminating the intrinsic comparator offset via input-referred offset storage (IOS) and preventing the dynamic offset from signal-dependent flipping DC level.

Owing to the nature of single-ended configuration, compared to differential configuration, the comparator is less immune to the noise from power supply and ground noise, and the operating current is dynamic due to no constant current bias. In this work, PMOS-input comparator is implemented to minimize cross-voltage of 3D-MIM capacitors with downward V_{RAMP} for reliability. As a result, the PMOS-input comparator is more vulnerable to the power supply noise. To improve the noise immunity of power supply, the on-chip low-dropout regulator (LDO) is implemented to ensure power quality. Besides, black level correction (BLC) in ISP is operated per frame to cancel the frame-wise fluctuation (lower frequency component of power supply and ground noise) by the means of optical black pixels operated in PD-ADC (PD-OB) and FD-ADC (FD-OB), accordingly and respectively. For the dynamic operating current, the clamp MOS is implemented to guarantee the comparator bias never cuts off. Moreover, the power supply voltage of ADC (1.1V core devices) is pushed down to 0.95V to minimize the transition current of 3Q logics and SRAM without performance degradation.

IV. Fixed Pattern Noise Correction

The FAU operation is illustrated in Fig. 4. The temporal noise (TN) of reference frames is suppressed by the recursive frame averaging, where the averaged frame counts can be programmed. Once the sensor power-on, the FAU initializes the consecutive PD-FPN-Ref frames and FD-FPN-Ref frames in sequence. To have consistent performance of various tracking applications and improve system stability, rolling updating triggered by temperature drift or certain frame count will trigger FAU to update reference frame memory with one PD-FPN-Ref frame and one FD-FPN-Ref frame with the programmable updating weight.

V. Sparse Transmission

The ST function supports sparse pixel readout to minimize the power consumption [8] in both sensor and system by only transmitting the necessary data. The selected pixels to be readout are programmed with a 200 × 200 × 1 bits compressed transmission map (TM) in the unit of 2 × 2 pixel cluster to save the packet size, transmission time, and decompression complexity. The compressed TM is sent to the sensor prior to the readout, and it is decompressed on the sensor before the

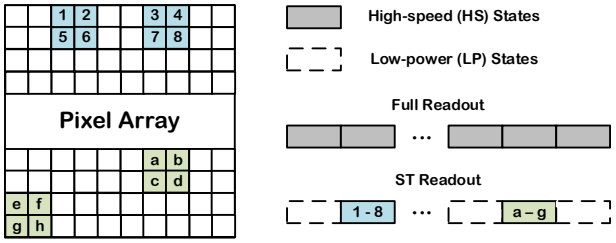

Fig. 5. The example of ST.

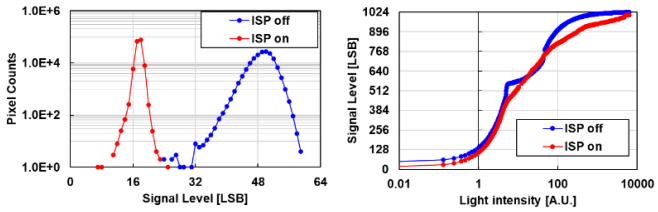

Fig. 6. The measured dark FPN and 3Q PRC.

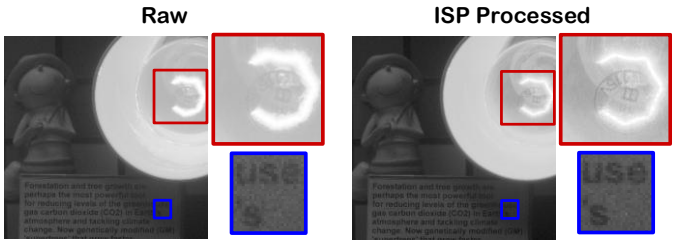

Fig. 7. The captured raw image (left, γ=0.5) and ISP processed image with FPNC (right, γ=0.5).

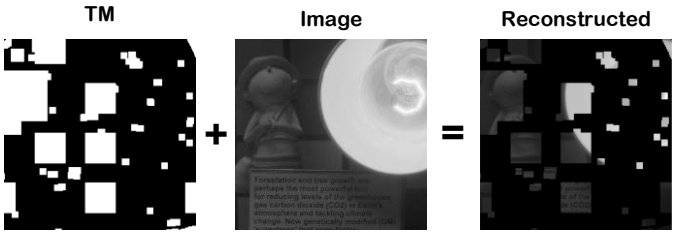

Fig. 8. The example of 25% ST reconstructed image.

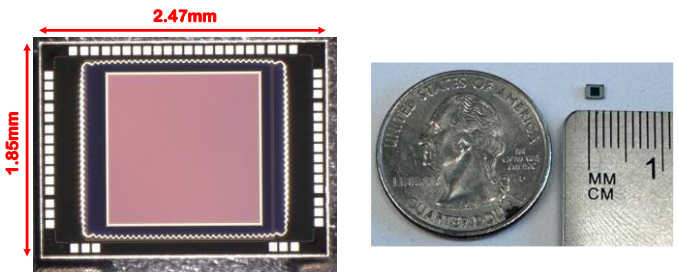

Fig. 9. Die photograph.

TABLE I

COMPARISON TABLE OF THE STATE-OF-THE-ART DPS

	This work Brillnics/Meta	TED 2022 [3] Brillnics/Meta	JSSC EA [4] Brillnics/Meta	SSCL 2024 [5] CSEM	JSSC 2022 [6] Samsung	JSSC 2018 [7] Sony
Process node [nm]	**45/40/40**	**45/65**	**45/40**	**65/40**	**65/28**	**90/65**
Supply voltage [V]	**2.6/1.8/1.1**	**2.5/1.8/1.2**	**2.5/1.8/1.1**	**1.8**	**2.8/1.05**	**2.9/1.1**
Pixel size [µm]	**3.24**	**4.6**	**3.96**	**6.3**	**4.95**	**6.9**
Resolution (H × V)	**400 × 400**	**512 × 512**	**640 × 640**	**640 × 480**	**1668 × 1364**	**1632 × 896**
In-pixel memory [bit]	**10**	**10**	**10**	**10**	**22**	**15**
Conversion gain [µV/e^-]	**208/19.4**	**170/7**	**108/7.7**	**N/A**	**132**	**60**
Linear full well [ke^-]	**5.5/18.7/3300***	**3.8/51/9000***	**2.6/36/10000***	**11000**	**7**	**16.6**
Noise floor [e^-_{rms}]	**4.4**	**4.2**	**6.4**	**11**	**4.6**	**5.15**
Dark FPN [e^-_{rms}]	**2.4**	**47**	**43.5**	**6**	**1.94**	**0.58**
Dynamic range [dB]	**117**	**127**	**124**	**120**	**63.6**	**70.2**
Power [mW]	**3.06 @ 30fps**	**5.75 @ 30fps**	**6.2 @ 30fps**	**1.33 @ 30fps**	**116.2 @ 30fps**	**746 @ 660fps**
FoM [e^-_{rms} × pJ]**	**0.0049**	**0.1809**	**0.0975**	**0.0021**	**6.06**	**1.24**

*** Equivalent full well.**

**** FoM = (power × noise)/(pixel resolution × frame rate × DRU); DRU = [(saturation/gain)/noise].**

readout starts. The sensor power saving with ST primarily results from the reduced power consumption for data transmission. Fig. 5 illustrates an example of packing sparse pixel clusters with ST function.

VI. MEASUREMENT RESULTS

The measured dark FPN and 3Q photon response curves (PRCs) are illustrated in Fig. 6. With ISP enabled, the dark FPN is improved from 2.4 LSB (10.7 e^-_{rms}) to 0.5 LSB (2.4 e^-_{rms}) by FPN-C with eight-frame averaging in FAU; The smoother conjunctions of (1) PD-ADC to FD-ADC and (2) FD-ADC to TTS are achieved. The captured raw image and ISP processed image with FPN-C are illustrated in Fig. 7 (enhanced gamma for better viewing). The FPN corrected and ISP processed image demonstrates improved dark noise when compared to the raw image and the functionality of HDR tone mapping by resolving the details in both the dark and bright regions. Fig. 8 shows an example of the 25% ST reconstructed image.

VII. CONCLUSION

Table I summarizes the performances of the reported DPS sensor and the state-of-the-art DPSs [3] – [7]. A 400 × 400 DPS with a 3.24µm pixel pitch, the smallest to date, is developed. A noise floor of 4.4 e^-_{rms} and dark FPN of 2.4 e^-_{rms} are achieved in 3Q operation. The sensor provides 117 dB DR in single exposure with a power consumption of 3.06 mW (FPN-C and ISP enabled) at 30 fps and 1 ms exposure time with the lowest figure of merit (FoM) of 0.0049 e^-_{rms} × pJ. The image processed by FAU and ISP enables more precise feature detection and optical character recognition (OCR). The ST feature further reduces power consumption for certain tracking applications. The sensor photograph achieves the extremely small die size of 2.47 × 1.85 mm^2 for the stringent camera module requirement of the AR/VR devices as illustrated in Fig. 9.

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